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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,894	09/28/2001	Phillip M. Jones	COMP:0239 P01-3650	3484

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Intellectual Property Administration
Legal Department M/S 35
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EXAMINER	
THAI, XUAN MARIAN	

ART UNIT	PAPER NUMBER
2111	4

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,894	JONES ET AL.	
	Examiner	Art Unit	
	XUAN M. THAI	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: -- MULTIPROCESSOR BUS COMPUTER SYSTEM HAS COHERENCY CONTROL MODULE INCLUDING ACTIVE SNOOP QUEUE MODULE TO FILTER SIMULTANEOUS MULTIPLE ACCESS REQUESTS TO SINGLE ADDRESS IN STATIC RAM --

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 8-12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donley et al. (USPN 5,822,611; Donley) in view of Merchant (USPN 5,893,151).

As per claims 1, 10 and 11, Donley discloses a computer system (fig. 1) comprising: a host controller (e.g. cache controller); a first processor bus (local processor bus) coupled between the host controller (cache controller) and a first processor (local processor); a second processor
bus (e.g. bus 50) coupled between the host controller (cache controller) and a second processor (processor(s) 1-a', 1-a"); a random access memory (1-M) coupled to the host controller via a memory bus (fig. 1), the RAM comprising a portion of static memory and a portion of dynamic memory; and a static RAM interface module configured to access an address look-up table corresponding to data stored in the static portion of the RAM (tag look-ups; col. 2, lines 1-23); and a coherency control (1-acc) module operably coupled to the first processor bus and the second processor bus and comprising: a request module configured to receive requests from the first processor bus and the second processor bus and to maintain proper ordering of the requests from each processor bus (e.g. col. 1, lines 64 et seq. bridging col. 2, lines 1-50). Donley also discloses requests ordering method, which uses cycle ID (col. 4, lines 15-27). However, Donley does not explicitly teach "an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM".

Merchant, in his system for maintaining cache coherency in a multiprocessor environment, teaches that a snoop queue 408 is used to maintain a list of requests currently

being processed and to prevent simultaneous multiple accesses to a single address in the cache (Abstract; see also fig. 4, col. 8, lines 9-67).

It would have been obvious to one of ordinary skill in the art to modify the coherency control of the Donley system to include the snoop queue module as taught by Merchant, in that Merchant states that such modification would allow ordering of requests to be properly tracked and resolve multiple conflicting snoop requests thus enhancing the overall performance of the system which depends upon the ability to share data in a coherent manner (col. 2, lines 1-20).

As per claim 2, the combination of Donley and Merchant discloses the computer system, as set forth in claim 1, further comprising an input/output (I/O) bus (Donley - col. 1, lines 50-56; and Merchant – col. 2, line 6, and col. 3, lines 24-38) coupled between the host controller and a plurality of I/O devices, wherein the I/O bus is operably coupled to the coherency control module and wherein the request module is configured to receive requests from the I/O bus (Donley - col. 1, lines 50-56; and Merchant – col. 2, line 6, and col. 3, lines 24-38).

As per claim 3, Donley discloses the coherency control module is located within the host controller (see fig. 1).

As per claims 4 and 12, the combination of Donley and Merchant discloses the computer system, as set forth in claim 1, wherein the coherency control module comprises a plurality of list structures (Merchant – col. 12, lines 5-9) corresponding to the first processor bus and the second processor bus.

As per claims 8 and 16, the combination of Donley and Merchant discloses the computer system, as set forth in claim 1, wherein the active snoop queue module comprises a plurality of active snoop queues, each active snoop queue configured to maintain a list of requests currently being processed and to function independently with respect to each other (Merchant - multiple snoop queues; col. 7, lines 22-31).

As per claims 9 and 17, the combination of Donley and Merchant discloses the computer system, as set for the in claim 1, wherein the static RAM interface module comprises a plurality of static RAM interfaces, each static RAM interface corresponding to a segment of the static portion of the RAM (plural caches; Donley – fig. 1; Merchant – fig. 1).

4. Claims 4-6 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Donley and Merchant as applied to claims 1 and 10 above, and further in view of McAllister et al. (US 20030200397; McAllister).

As per claims 4-6 and 12-14, the combination of Donley and Merchant does not explicitly teach the specific of the list structures as claimed. However, McAllister, in his memory control system including cache coherency control, teach that it is known to provide a plurality of list structures (doubly-linked lists; fig. 5) with head and tail pointers (head and tail flags) and dependency links (e.g. para. [015], [018], [027]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory control of Donley to include a plurality of linked list structures as taught by McAllister, in that McAllister teach that the linked list structures as disclosed would memory controller to enable proper ordering of requests to a shared memory in a multiprocessor system and to maintain coherency.

Therefore, the modification would enhance overall system performance in addition to being significantly easier to design and verify, thereby minimizing development costs and minimizing time to market (para. [029]).

5. Claims 4-7 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Donley and Merchant as applied to claims 1, 4, 10 and 12 above, and further in view of VanDoren et al. (US 6279084; VanDoren).

As per claims 4-7 and 12-15, the combination of Donley and Merchant teaches the claimed invention with respect to claims 1, 4, 10 and 12, above but does not explicitly teach linked list buffers, dependencies and bypass paths configured to provide a direct request path from the first and second processor buses to the static RAM interface module, thereby bypassing the list structures as claimed.

VanDoren, in his memory coherency control system, teach that it is known to provide linked list buffers, dependencies (cols. 22-30) and bypass path for direct reading of the memory system (col. 12, lines 5-12). It would have been obvious to one of ordinary skill in the art to modify the Donley memory controller to include linked list buffers, dependencies and bypass path for providing direct request path to the memory system when there is no other requests pending as taught by VanDoren. VanDoren states that using a linked list buffering scheme, where ordering dependencies are accommodated through the use of multiple queues that store flags and where the queues are selected to identify dependencies in addition to using bypass path in the data transmitting scheme, the complexities of operations that are performed by a manager

to maintain order and ensure coherency while maximizing bus utilization is simplified (col. 30, lines 35-54).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

XUAN M. THAI
Primary Examiner
Art Unit 2111

XMT